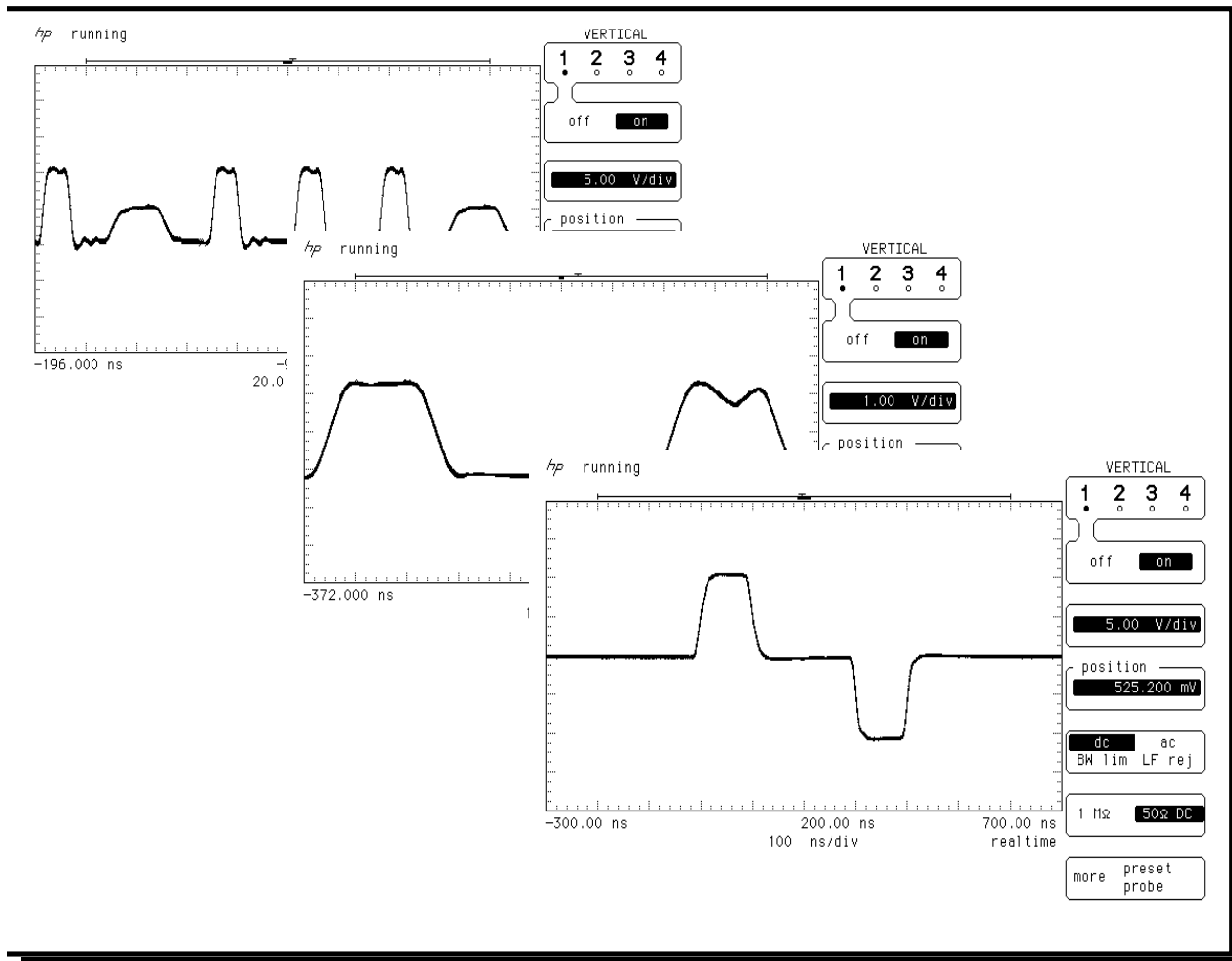


---

# How To Generate Real World Signals With the HP 8110A










---

## Product Note 8110A



**"Digital Design and Test  
Solutions from HP"**

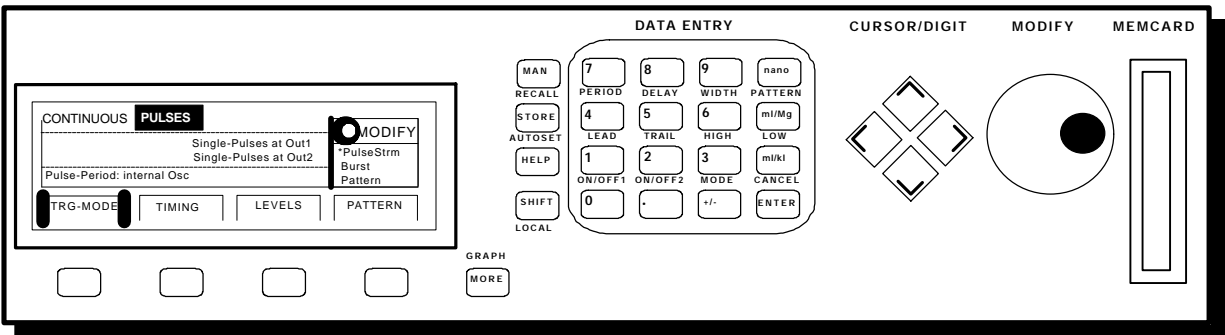
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## Getting Started with the HP 8110A

### A. Front panel tour

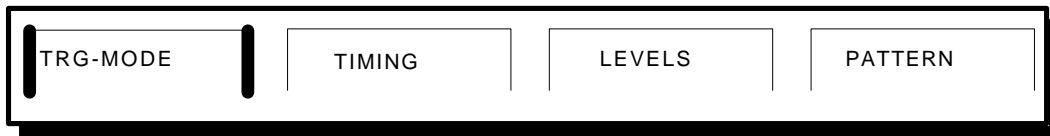


1. Move the parameter cursor using the **CURSOR** keys. The selected parameter is shown in the Modify Window at the right side of the display. Use the **SHIFT CURSOR** keys to select a DIGIT or increment/decrement a DIGIT in the Modify Window.
2. Modify the parameter/menu selection in the Modify Window using the **MODIFY** knob.
3. Select a parameter screen using the Softkeys and **MORE**. Use **SHIFT MORE** or press a softkey twice to toggle from the text display to the graphical display, when available.
4. Use the **DATA ENTRY** keys to type a value directly into the Modify Window or select a commonly used parameter quickly using the **SHIFT** functions above the keys.
5. Use a plug-in **MEMORY CARD** to store and recall instrument settings or update firmware. You can also store/recall instrument settings to/from memory locations 1 -9 in the instrument's nonvolatile memory by using the **STORE/RECALL** keys.



## B. Parameter keys

All of the parameters and settings which control the HP 8110A are available on one of up to eight parameter screens. The parameter screens group together parameters which are most likely to be used together.



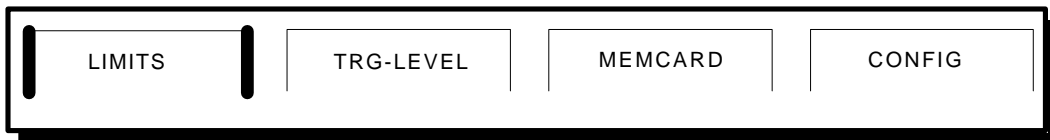
**TRG-MODE**      The overall operating modes of the instrument - triggering, pulse types, period and triggering sources.

**TIMING**      All the pulse timing-parameters for Outputs 1 and 2.

**LEVELS**      All the pulse voltage or current levels and impedances for Outputs 1 and 2.

**PATTERN**      4096 bit pattern data (for each channel output and STROBE OUT).

**Press the MORE key to view the next level**

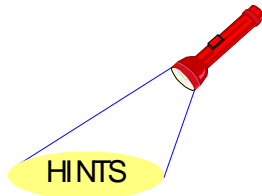


**LIMITS**      Voltage and current limits (for both outputs if installed).

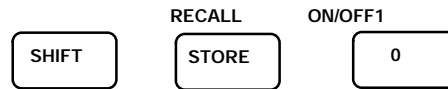
**TRG-LEVEL**      EXT INPUT, STROBE OUT, Trigger OUT and CLK IN levels and impedances.

**MEMCARD**      Memory card operations.

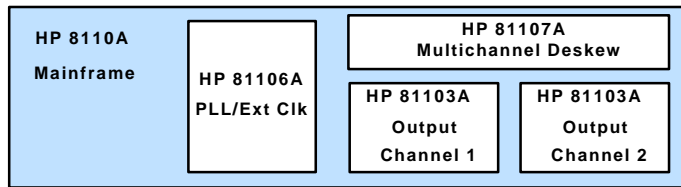
**CONFIG**      General instrument configuration- HP-IB address, deskew (if installed) and parameter grouping.



- Before you set up any application, we recommend that you recall the standard parameters to always begin from the same settings by pressing:



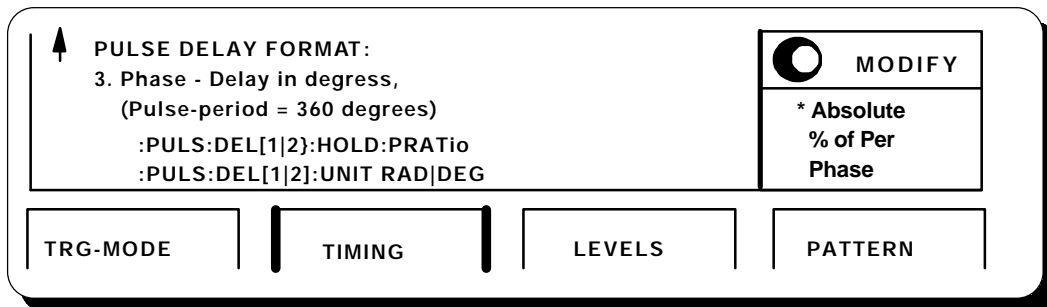
- To identify what modules (81103A, 81106A, 81107A) are installed in your HP 8110A mainframe, what the serial numbers are, or what revision of the firmware is installed:



Press **HELP** followed by the **SERIAL #** softkey and scroll with the **MODIFY** knob.

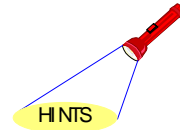
- If you get a flashing **W** (Warning) or flashing **E** (Error) at the bottom of the HP 8110A screen, press **HELP** to see a short explanation of the current Warning/Error message.
- If there are no flashing Warnings or Errors, press the **HELP** key at anytime to get information about the currently highlighted parameter. This information includes such things as a short description, range specifications, and/or the SCPI programming command.

For example if **Delay** is highlighted on the **TIMING** menu, the **HELP** menu displays:

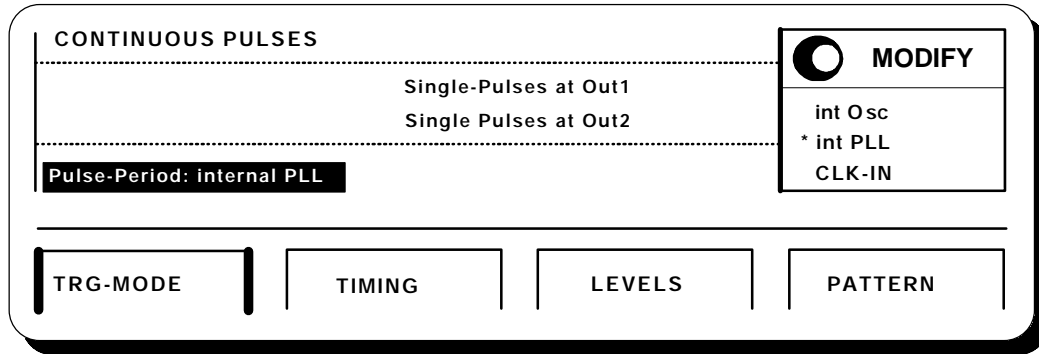


Scroll up for the rest of the information using the **MODIFY** knob.

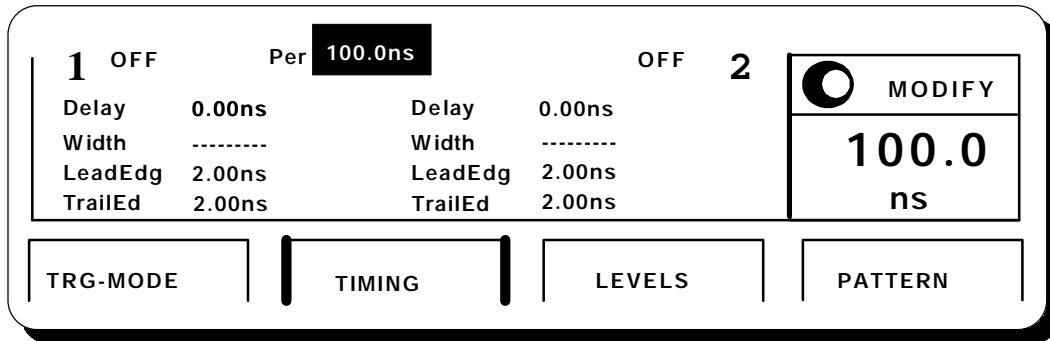
5. If the HP 81106A PLL/External Clock Module is installed:



- A. The TRIGGER menu includes the choices  
**Pulse-Period: internal PLL** for higher period accuracy and lower jitter, and  
**Pulse-Period: external CLK-IN** for the period to be synchronized to the rising or falling edge of an external input signal to the PLL REF/CLK IN rear BNC input connector.

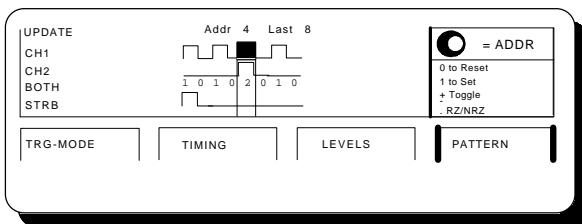


- B. The TIMING menu's **Freq/Per** displays 4 digits of resolution if the **Pulse-Period: internal PLL** is selected on the TRIGGER menu.

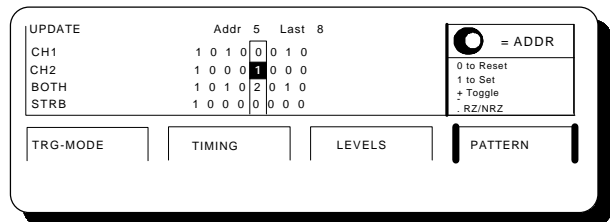


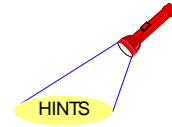
6. Toggle the menu softkey (TIMING, LEVELS, or PATTERN) to display the graphical or textual version of that menu on the HP 8110A.

**Graphical**

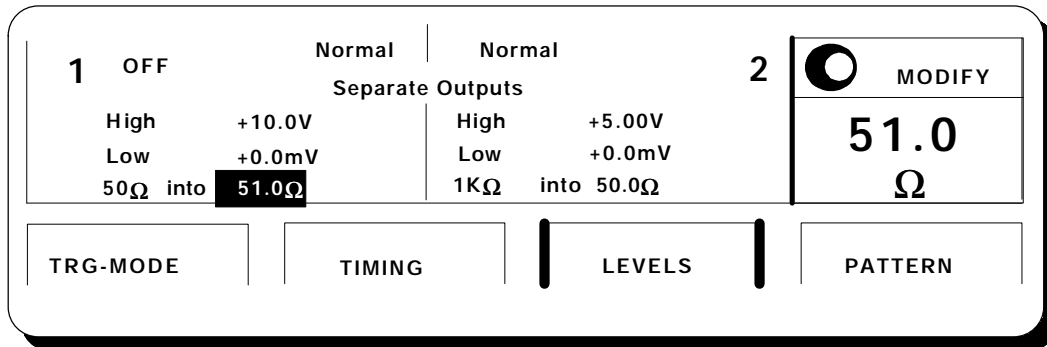


**Textual**





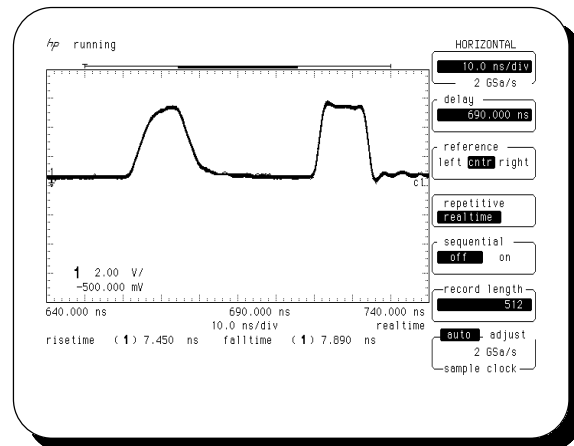
7. If you cannot enter the requested voltage, check to see if you have the correct Source and Load impedances selected on the LEVELS menu.



8. If you are using the internal channel addition, **Added at Output 1** selected on the LEVELS menu, then please be aware that the edge rates of the signal from channel 2 will slow down when added internally.

In the scope picture to the right, the first pulse is from channel 2 and the second pulse is from channel 1.

### Added at Output 1

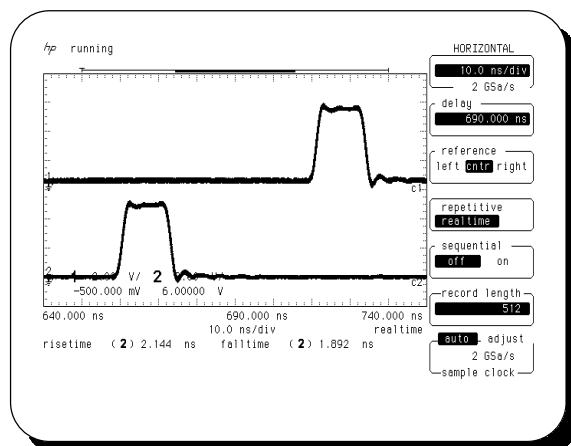


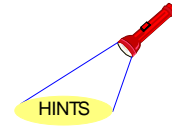
If this is a problem, then choose **Separate Outputs** and add the two outputs externally to maintain the originally selected edge rates from channel 2.

In the scope picture to the right, the top waveform is from channel 1 and the bottom waveform is from channel 2.

See typical specifications in the data sheet for details.

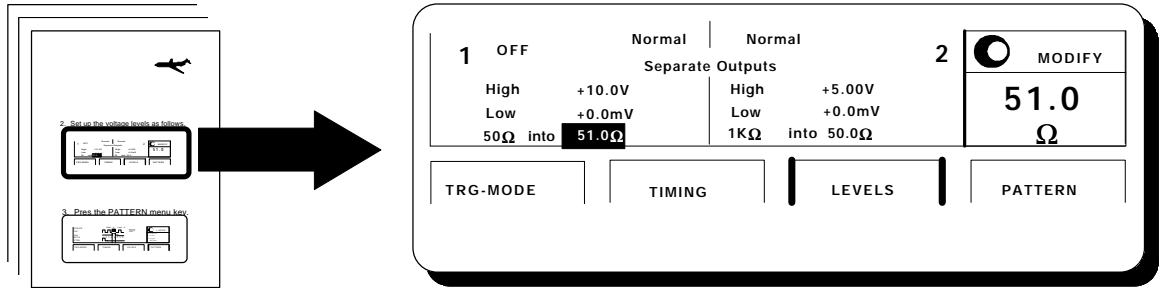
### Separate Outputs





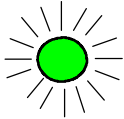
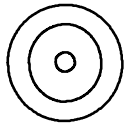
## 9. If you aren't getting the correct HP 8110A output signals displayed on the scope:

- A. Are all of the parameter selections shown in the setup step pictures completely duplicated on your HP 8110A menu displays?



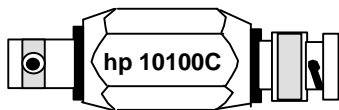
- B. Have you turned ON the Output(s) from the LEVELS or TIMING menu?

### OUTPUT 1



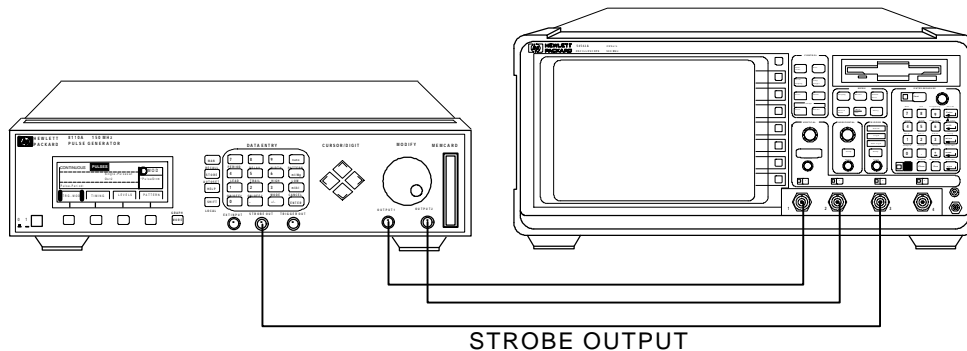
If the Output is ON, the green light next to the front panel BNC connector will also be ON.

- C. Is the scope input impedance set to 50  $\Omega$  DC? Or if you don't have that selection on your scope, do you have a 50  $\Omega$  Ohm feedthrough connector at the input to the scope?

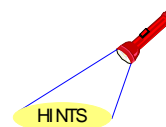


**50 $\Omega$  Feed Through Termination**  
DC - 300 MHz VSWR Max. 1,1


- D. Are you triggering the scope from the HP 8110A's Strobe Output Channel?



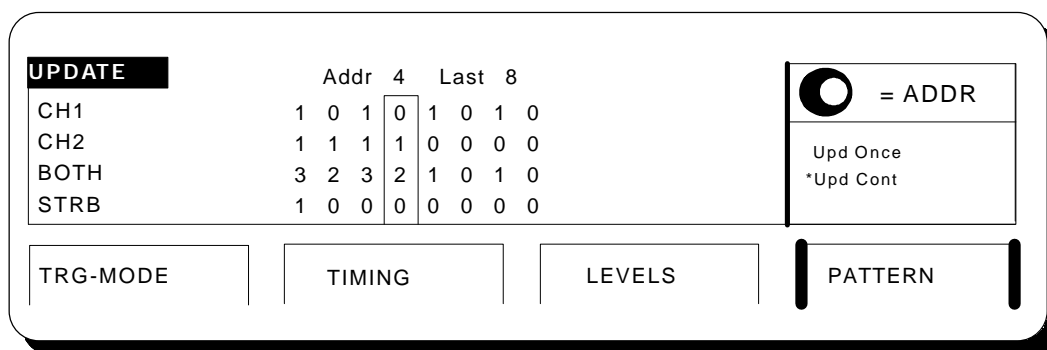







### 10. An easy step-by-step way to enter patterns in the PATTERN menu:

A. Press the **PATTERN** softkey and use the cursor (arrow)  keys to move around the menu and highlight **UPDATE**.

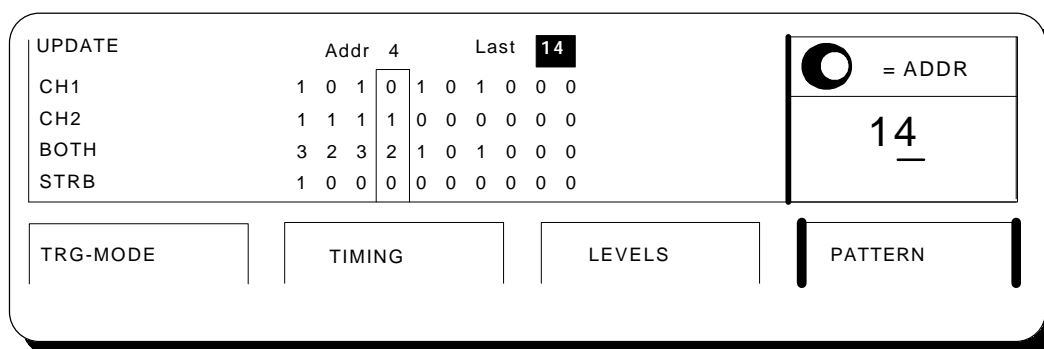
Then use the **MODIFY** knob and select **\* Upd Cont** to make sure the pattern is updated to the outputs continuously (realtime).

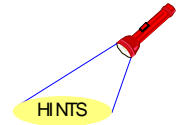


B. Highlight the value to the right of **Last** to set the length of your desired pattern between

2 and 4096 bits. You can enter the length using the Data Entry keys (    )

or the **MODIFY** knob.





C. Use the cursor keys to highlight the bit in the CH1 row positioned directly underneath the **Addr** value. Notice this bit is outlined by a box.

Use the **MODIFY** knob to change the active (boxed) bit to **Addr 1**.

UPDATE	Addr 1	Last 14
CH1	<b>1</b>	0 1 0 1 0 1
CH2	1	1 1 1 0 0 0
BOTH	3 2 3 2	1 0 1
STRB	1	0 0 0 0 0 0

=ADDR  
 0 to Reset  
 1 to Set  
 + Toggle  
 - RZ/NRZ

TRG-MODE
TIMING
LEVELS
PATTERN

D. Now you are ready to begin entering your pattern in CH1.

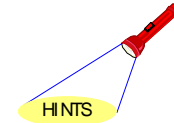
Press Data Entry key  or . Notice after entering a 1 or 0 the active bit moves to the next consecutive address. For example, with a 14 bit pattern, begin at **CH1 Addr1** and enter: **1 0 1 1 0 1 1 1 0 1 1 1 1 0**

Experiment with the  key to toggle a bit; in this case the active bit does not move.

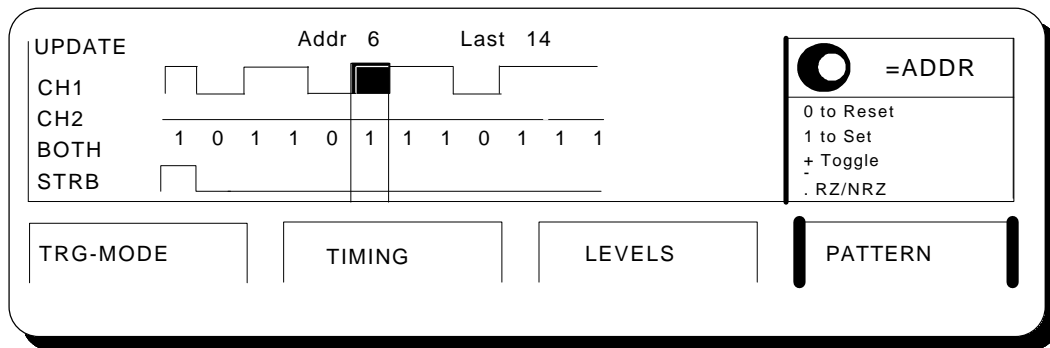
UPDATE	Addr 14	Last 14
CH1	0 1 1 1 1 <b>0</b>	
CH2	0 0 0 0 0 0	
BOTH	0 1 1 1 1 0	
STRB	1 0 0 0 0 0	

=ADDR  
 0 to Reset  
 1 to Set  
 + Toggle  
 - RZ/NRZ

TRG-MODE
TIMING
LEVELS
PATTERN



E. Toggle the **PATTERN** softkey to see the resulting signal of 4 pulses with growing pulse widths.

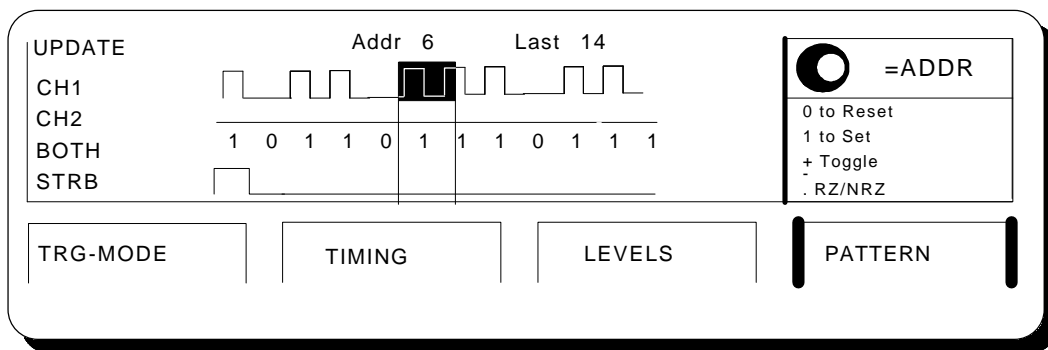


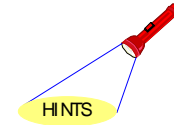
If you see 10 pulses of equal pulse widths you are in the RZ display mode.

Toggle the **.** key while in the graphical **PATTERN** menu to see what the waveform will look like in either the RZ (Return-to-Zero) format or NRZ (Not-Return-to-Zero) format.

**Note:** This decimal key does not physically change the format at the output.

Only the **TRG-MODE** menu selections **RZ-Pulses at Out1(2)** and **NRZ-Pulses at Out1(2)** actively change the format of the pattern at the output(s).





11. If you wish to save the HP 54542A scope waveforms you capture on your display to a 3.5" disk:

A. Insert a 3.5" disk in the disk drive.

B. Press the blue  shift key and the  Wform save key.

C. If the disk is not yet formatted, press  format  LIF  DOS  execute  exit menu .

D. Select  store image and select the highlighted choices as shown below.

```

file suffix nn = 00 - 99,
incremented on each store

autoincrement reset to OFF
and suffix nn reset to 00
when this menu reentered
    
```

DOS Filename	Date	Time	Bytes	File Description
HINTS00 .TIF	4May94	6:00:34	7308	DOS FILE - NO DESC
HINTS01 .TIF	4May94	6:02:24	7186	DOS FILE - NO DESC
HINTS02 .TIF	4May94	6:02:36	7186	DOS FILE - NO DESC
HINTS03 .TIF	4May94	6:02:42	7593	DOS FILE - NO DESC
HINTS04 .TIF	4May94	6:02:56	7186	DOS FILE - NO DESC
HINTS05 .TIF	4May94	6:03:20	7186	DOS FILE - NO DESC

```

DOS Disk Space(bytes) - Total: 1474560 Free: 1384448
    
```

STORE IMAGE

disabled  enabled

format

TIFF  PCX  EPS

compression

on  off

rendering

B/W  gray  green

to files

[HINTS0nn]

bytes: ~12K

autoincrement

off  on

exit menu

E. exit the menu

F. Press another key (for example a channel key  1 ).

G. Capture the waveforms you want on the screen and then press  Print .

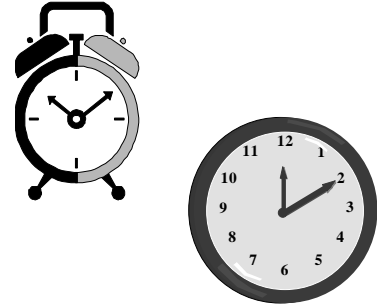
H. The following messages will be displayed as it is storing to the disk:

- "formatting image"
- "printing image to disk"
- "screen image stored to file HINTS01.TIF"

**Note:** Each time you print it will increment the filename since auto increment is enabled.

## Dual Clock GBit Chip Test

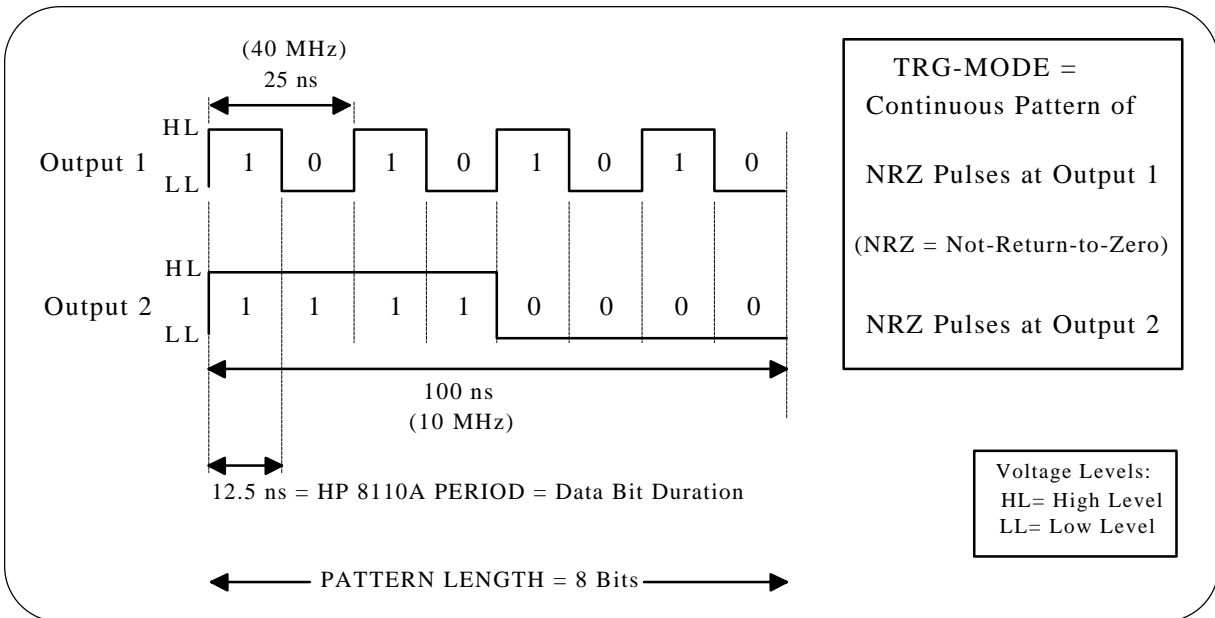
**Industry/Application Area:**  
Semiconductor Test Clocks and Digital  
Communication Clocks.



**Overview:**

Many customers need the ability to generate more than one clock signal simultaneously and at multiple frequencies. The HP 8110A is a perfect fit for functional test of the GBit Chip in the dual clock mode. Using the HP 8110A's pattern capability it is easy to create the necessary clock signals, one at 40 MHz and the other at 10 MHz. With their additional clock requirement of 0.1% frequency accuracy, the HP 81106A is a necessary module addition; without this module the frequency accuracy is a standard  $0.5\% \pm 100$  ps. By varying the frequency, duty cycle (pulse width as a % of period), and delay of the dual clocks, the HP 8110A can also be used to characterize timing margins of the chip, e.g. maximum toggle frequency, minimum and maximum duty cycle, and maximum clock-to-clock skew before failure.

**Timing Diagram of HP 8110A Dual Clock Signals:**





**Setting up the HP 8110A:**

1. Select NRZ-PULSES at OUT 1& 2 in the TRG-MODE menu.

2. Set up the following bit pattern in the PATTERN menu.

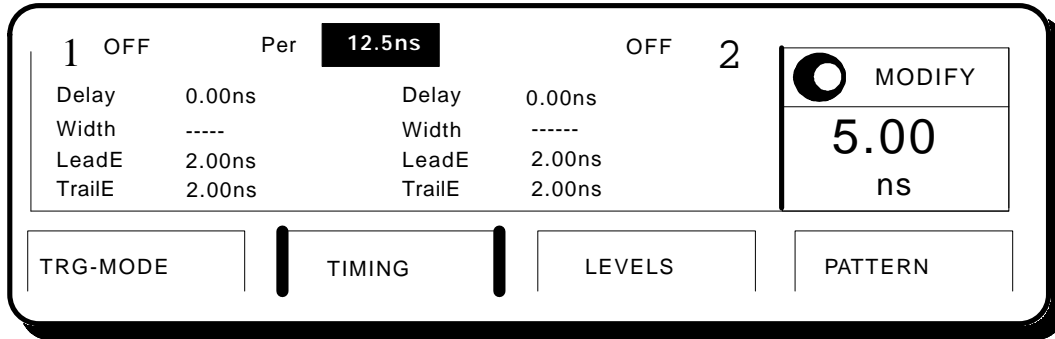
UPDATE	Addr 4	Last 8
CH1	1 0 1 0	1 0 1 0
CH2	1 1 1 1	0 0 0 0
BOTH	3 2 3 2	1 0 1 0
STRB	1 0 0 0	0 0 0 0

3. Press the PATTERN key again to view the pulses.

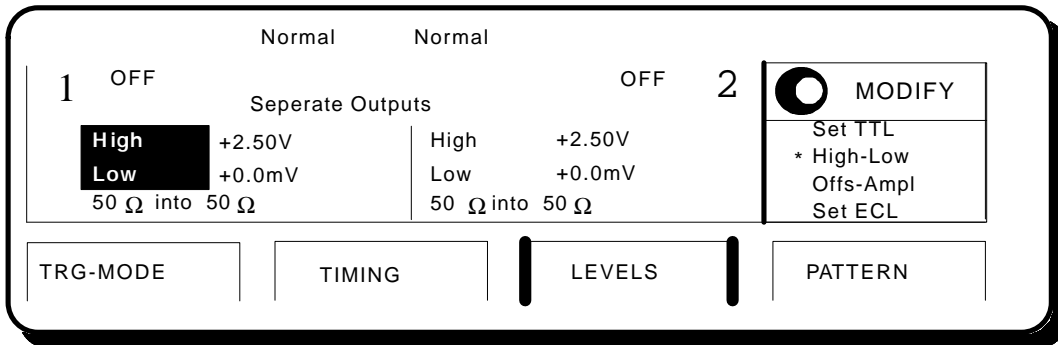




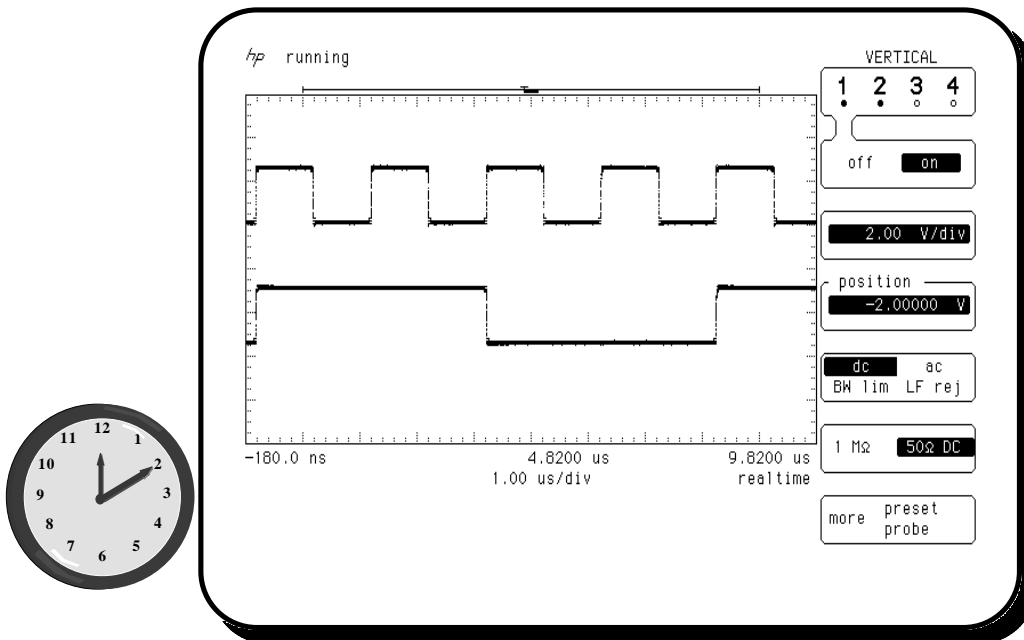
4. Set the period to 12.5 ns. The period is the duration of a single data bit when in the PATTERN mode.



5. Go to the LEVELS Menu to set the appropriate clock output voltages.

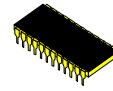


6. Here is the HP 54542A Scope display of the two different frequency clock signals generated by the HP 8110A.





# Flash Memory Cell Endurance and Performance Test



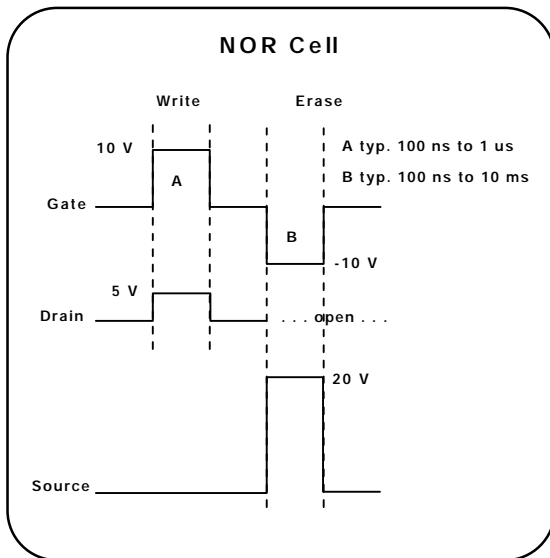
## Industry/Application Area:

IC Manufacturers, Computer Manufacturers/R&D, Reliability, Production

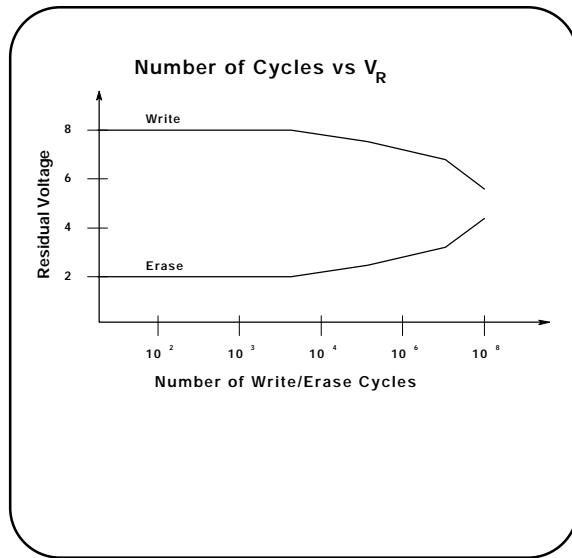
## Overview:

Flash EEPROMs potentially replace EPROMs, EEPROMs, floppies and hard disks because of their lower cost. To make the F-EEPROM a commercial proposition, they need to be sufficiently fast and have a long life span. However, the faster the operation and the more the program/erase cycle is performed, the less distinct thresholds become. Consequently, pulse-width/threshold and operating-cycles/threshold measurements are vital in flash memory test.

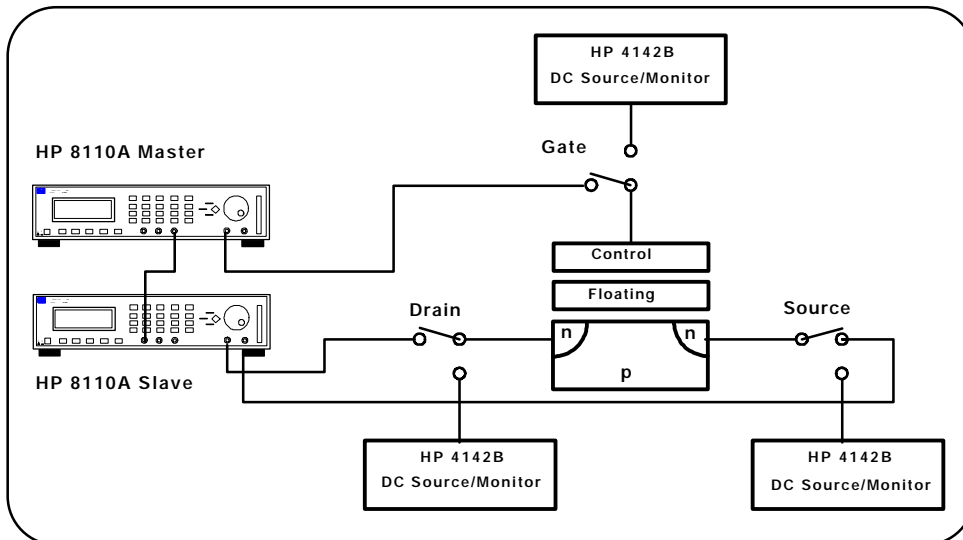
### Write / Erase Pulses



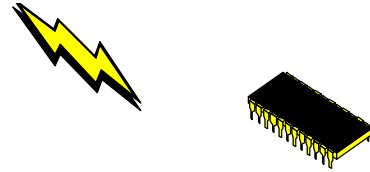
### Memory Cell Life



### Block diagram of test set-up







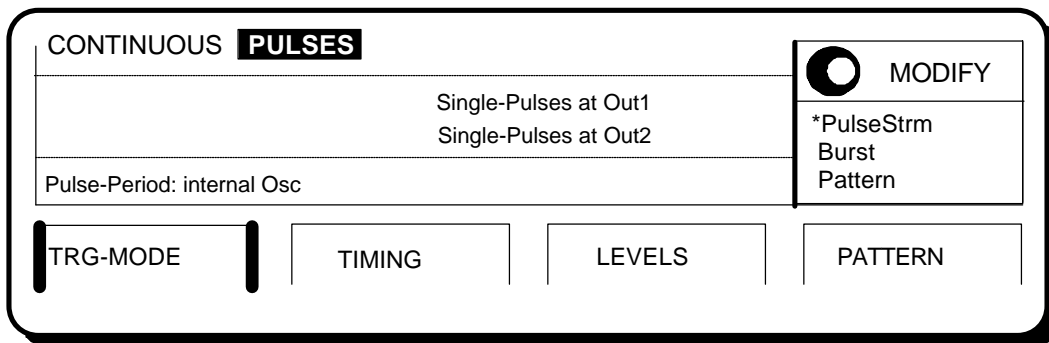
### Measurement Task:

1. Reduce the pulse width necessary for adequate distinction between write and erase thresholds (i.e. improve operating speed).
2. Characterize number of operations before "fatigue" causes thresholds to merge.

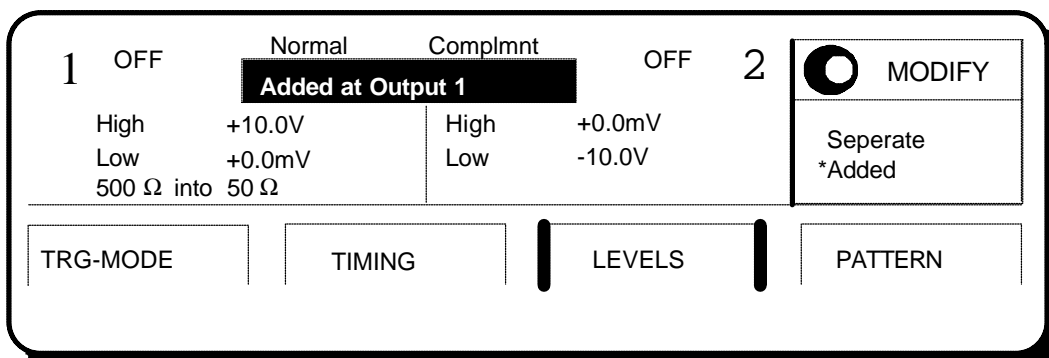
*NOTE:* The 8110As bipolar 3-level signals go up to 14 V for a symmetrical signal from 50-ohm into 50-ohm. Although not necessary in this system, two 8114As could be used to provide these signals if higher voltages are needed. We understand some flash memories need unipolar signals in excess of 20 V; again, the 8114A could solve these situations.

### Setting up the HP 8110A Gate Signal (Master box):

1. Select **SINGLE-PULSES AT OUT 1 & 2** using the **MODIFY** knob in the **TRG-MODE** menu.

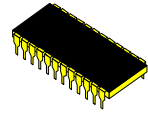


2. Set the **HIGH** and **LOW** levels, add the two channels together, then complement channel 2 and set the source impedance to 500 ohms



in the **LEVELS** Menu.

3. If the deskew module, HP 81107A is not installed, add delay to both channels to compensate for the prop delay between the master and slave boxes. Then add another 300ns of delay to channel 2 to position the negative going Erase pulse.



1 OFF Per 1.00us

Delay	21.0ns	Delay	321.0ns
Width	100ns	Width	100ns
LeadEdg	10.0ns	LeadEdg	10.0ns
TrailEd	10.0ns	TrailEd	10.0ns

2  MODIFY  
1.00 us

TRG-MODE | TIMING | LEVELS | PATTERN

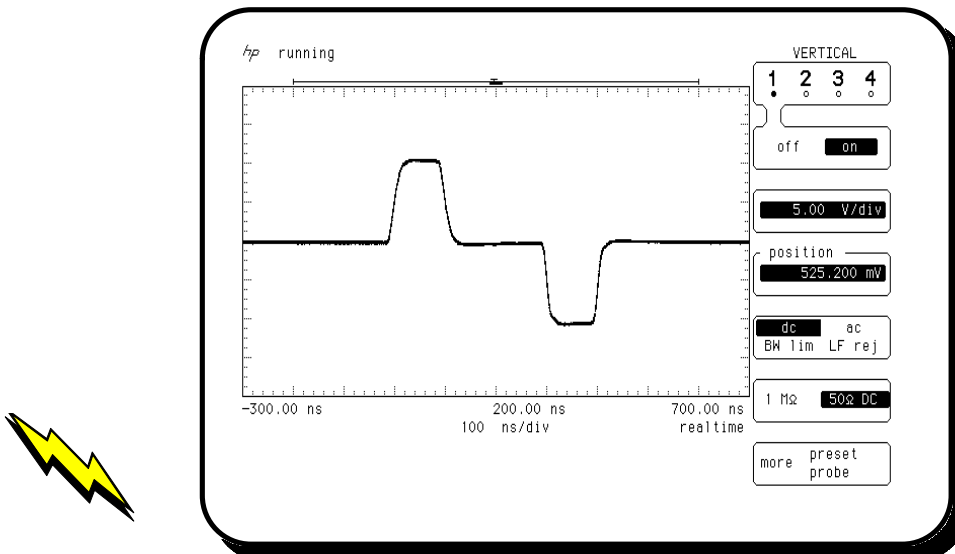
4. If the deskew module is installed, the prop delay can be compensated for in the CONFIG menu.

HPiB Address: 22  
Perform Selftest: uP Board  
Group Params by: TIMING / LEVELS  
PLL - Ref : Internal  
Deskew 1 : 21.0ns 2 : 21.0ns

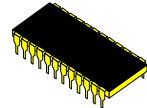
MODIFY  
21.0 ns

LIMITS | TRG-LEV | MEMCARD | CONFIG

5. Here is the HP 54542A display of the Write and Erase pulses generated by the HP 8110A.



Setting up the HP 8110A Drain and Source signals (Slave box):



1. Set up the second box to be triggered by a signal at the external input.

TRIGGERED

PULSES

MODIFY

---

Single-Pulses at Out1  
 Single-Pulses at Out2

---

Trg'd by: EXT-IN

Continuous  
 \*Triggered  
 Gated  
 Ext-Width

---

TRG-MODE

TIMING

LEVELS

PATTERN

2. Set up the Drain and Source signals equivalent in width to their respective Write and Erase signals.

1

OFF

Per -----

2

MODIFY

---

Delay	0.00ns	Delay	300ns
Width	100ns	Width	100ns
LeadEdg	10.0ns	LeadEdg	10.0ns
TrailEd	10.0ns	TrailEd	10.0ns

---

TRG-MODE

TIMING

LEVELS

PATTERN

3. Go to the LEVELS Menu and set the Drain and Source levels.

1

OFF

Normal      Normal  
Separate Outputs

2

MODIFY

---

High	+5.00V	High	+19.4V
Low	+0.0mV	Low	+0.0mV
50 Ω to	50.0 Ω	1K Ω into	50.0 Ω

---

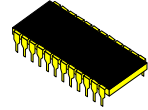
TRG-MODE

TIMING

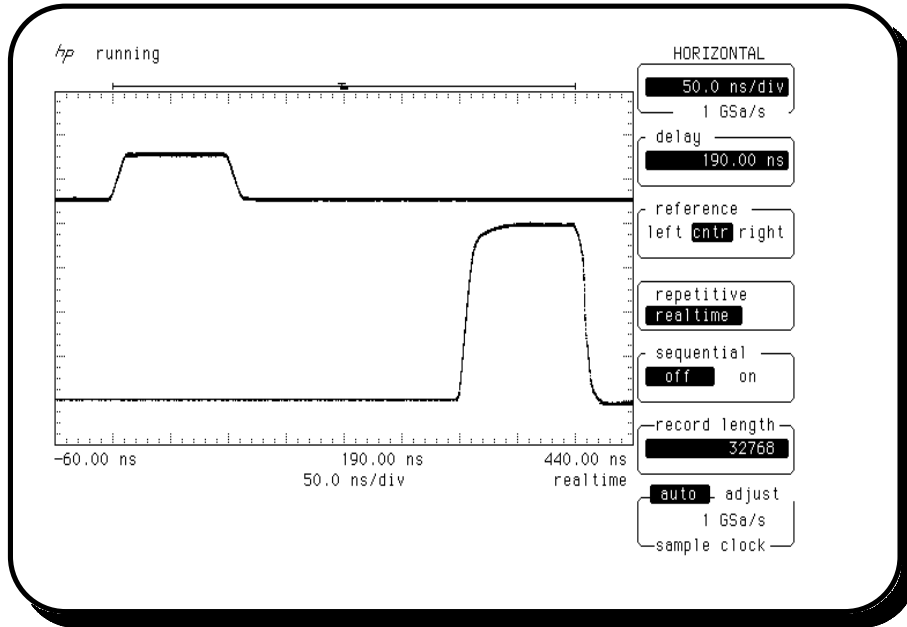
LEVELS

PATTERN





4. Here is the HP 54542A Scope display of the Drain and Source Pulses generated by the HP 8110A.



## Development of New AIRINC Bus

### Industry/Application Area:

Communications/R&D of Bus and Receiver



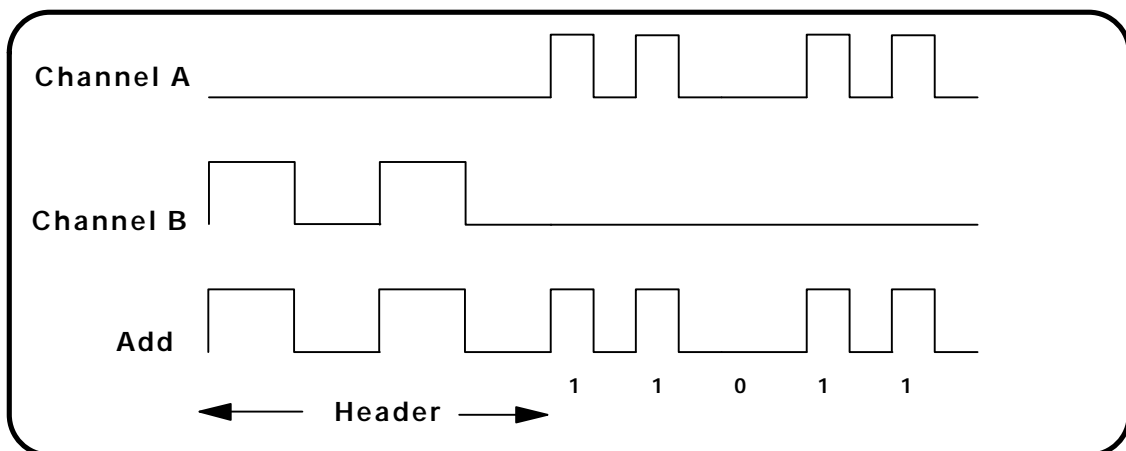
### Overview:

The bus requires data packed into two bytes preceded by a header. A peculiarity of the code is that the header consists of double bits that look like NRZ format while the data is in RZ.

How do you simulate this mix? One way is to set up a data generator using two bits for each emulated RZ bit (00=0, 10=1), and four bits for each header bit. Problems: You need twice as many generator bits as real bits, and, the data generator must run twice as fast to keep up with the real data rate!

The 8110A's Add mode gets around this problem elegantly because RZ data is programmed in one channel and NRZ in the other. This way, the full 4-k memory is available for application bits.

### Timing Diagram of LAN Stimulus:





**Setting up the HP 8110A:**

**1. Set Channel 1 for RZ pulses and Channel 2 for NRZ pulses.**

CONTINUOUS PATTERN of

**RZ-Pulses at Out1**  
NRZ-Pulses at Out2

Pulse-Period: internal Osc

MODIFY  
\* RZ  
NRZ

TRG-MODE | TIMING | LEVELS | PATTERN

**2. Set up the bit pattern as shown below.**

UPDATE                      Addr 5    Last 9

CH1	0	0	0	0	<b>1</b>	1	0	1	1
CH2	1	0	1	0	0	0	0	0	0
BOTH	2	0	2	0	1	1	0	1	1
STRB	1	0	0	0	0	0	0	0	0

= ADDR  
0 to Reset  
1 to Set  
+ Toggle  
. RZ/NRZ

TRG-MODE | TIMING | LEVELS | PATTERN

**3. Press the PATTERN Menu key again to view the waveforms.**

UPDATE                      Addr 5    Last 9

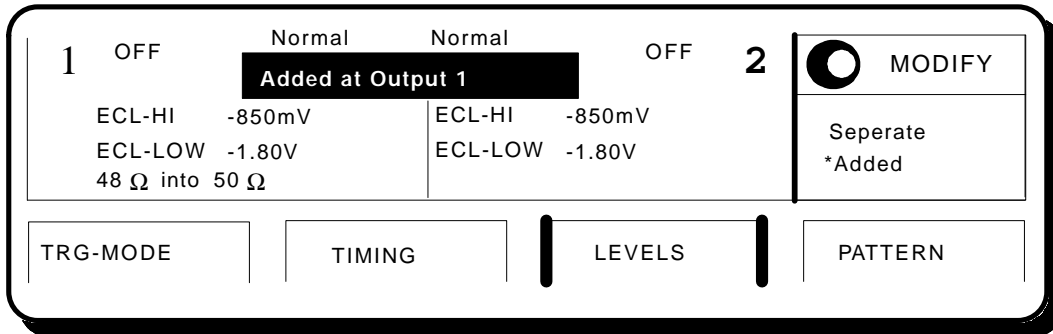
CH1										
CH2										
BOTH	2	0	2	0	<b>1</b>	1	0	1	1	
STRB										

= ADDR  
0 to Reset  
1 to Set  
+ Toggle  
. RZ/NRZ

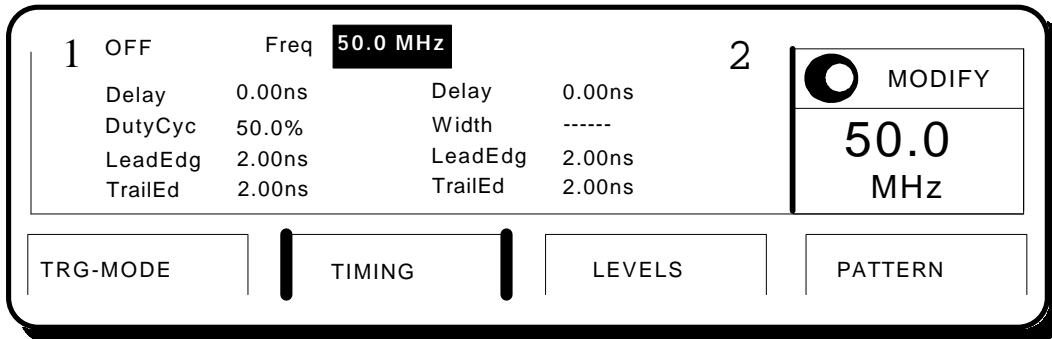
TRG-MODE | TIMING | LEVELS | PATTERN



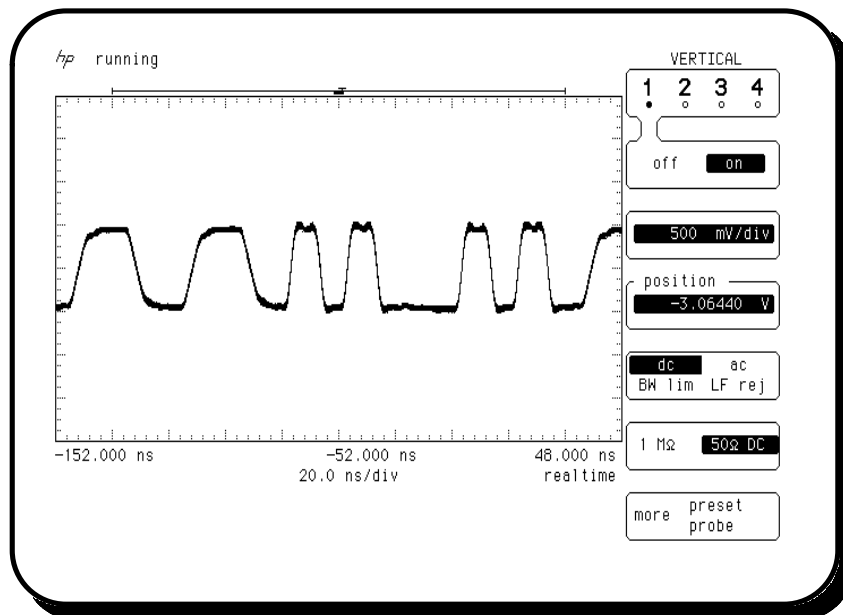
4. Now go to the LEVELS Menu to add the channels together.

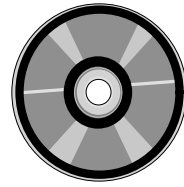


5. Set the frequency of the header and data to 50 MHz.



6. Here is the HP 54542A Scope display of the header and data generated by the HP 8110A.





## Magneto-Optical Disk Drive Research

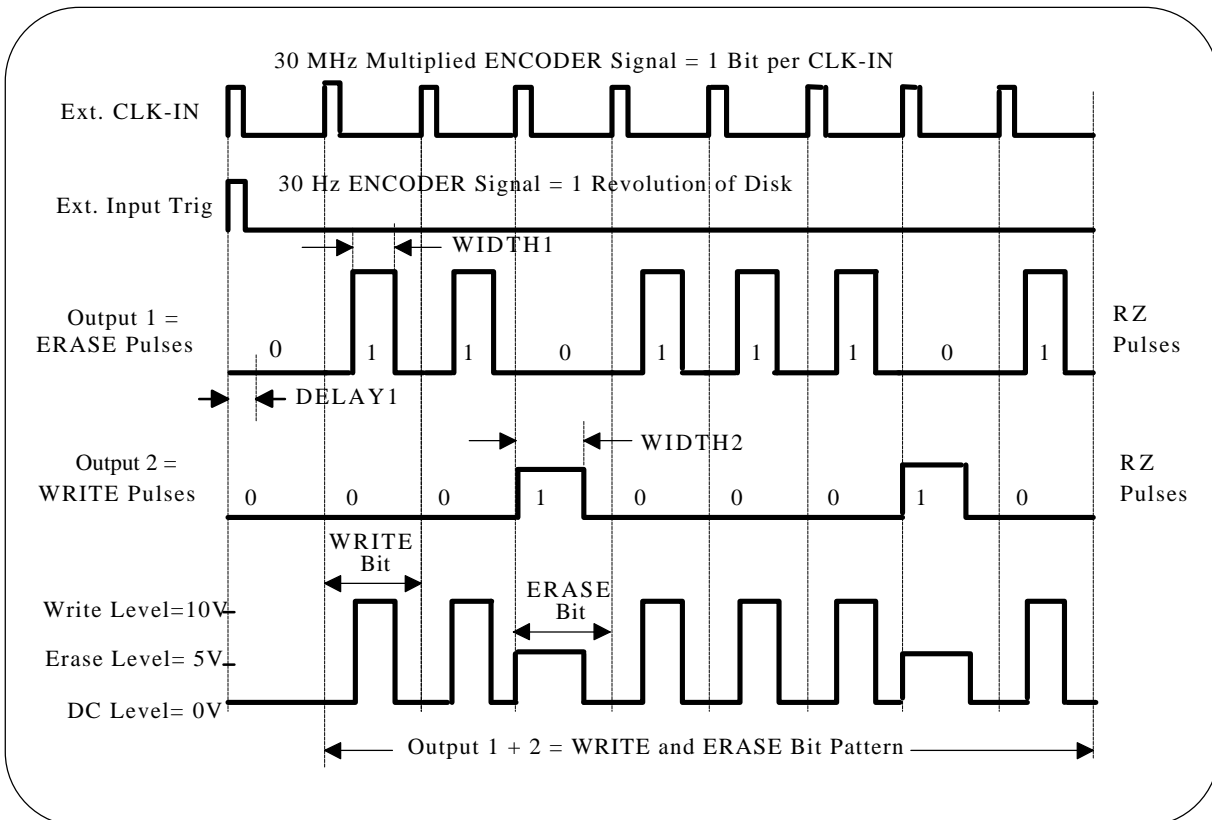
### Industry/Application Area:

Computers/Research of CD Rom (Magneto-Optical Disk) Technology

### Overview:

The customer is trying to write and erase a bit pattern to an MO (magneto-optical) disk by pulsing a laser at different write and erase voltages and pulse widths. The customer wants to experiment with writing and erasing over the same spot on the disc per every disk revolution. "Writing" places a "1" on the disk; this orients the magnetic fields at that spot (position) in a specific direction. "Erasing" places a "0" on the disk and orients the magnetic fields in the opposite direction. By creating the write pattern on one channel and the erase pattern on a second channel, it is easy to independently vary the voltage levels and pulse widths and then combine them into one pulse pattern at Output 1 via channel addition.

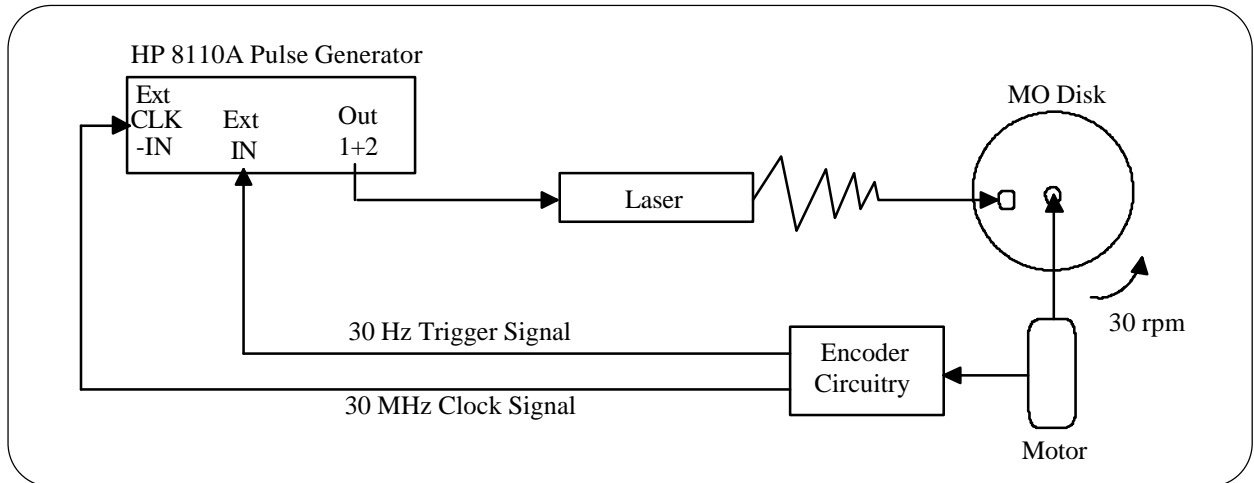
### Timing Diagram of Write and Erase Bit Pattern:







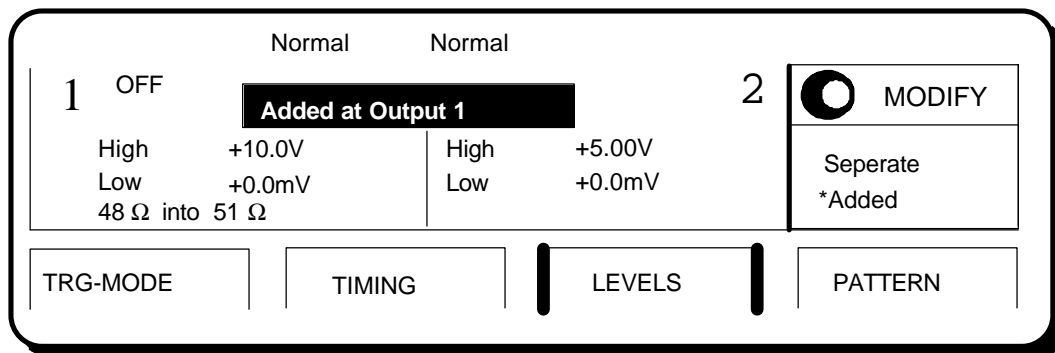
The MO disk is rotated by a motor which runs at 30 Hz. Because the motor may speed up or slow down at any given time, the biggest problem is in finding the exact same spot on the disk to write or erase over. The critical requirement is therefore extremely accurate and



repeatable edge placement of the pattern with respect to the position on the disk per disk revolution. An encoder is attached to the motor to provide a clock signal which is synchronized to the rotation speed of the motor. This clock signal is fed into the HP 8110A to maintain position repeatability on the disk from revolution to revolution. The external clock signal is multiplied up from 30 Hz to 30 MHz in order to run at the same frequency as the desired write/erase data rate to the disk. The HP 81106A PLL/Ext. Clock module is required in this mode, since it adds the External Clock Input capability to the generator. As seen in the timing diagram above, two synchronized encoder pulses are required to trigger the pattern to begin and clock each bit of the pattern.

### Setting up the HP 8110A:

1. Set the **WRITE** voltage levels on channel 1 and the **ERASE** levels on channel 2. Then using the **MODIFY** knob select the outputs to be **ADDED AT OUTPUT 1**.





2. Select **CONTINUOUS PATTERN** of and **RZ-PULSES AT OUTPUT 1 & 2** using the **MODIFY** knob in the **TRG-MODE** menu.

CONTINUOUS PATTERN of		<input checked="" type="radio"/> MODIFY * RZ NRZ
RZ-Pulses at Out1 RZ-Pulses at Out2		
Pulse-Period: internal Osc		
TRG-MODE	TIMING	LEVELS
PATTERN		

3. Set the **WRITE**, **ERASE** and **DELAY** values in the **TIMING** menu.

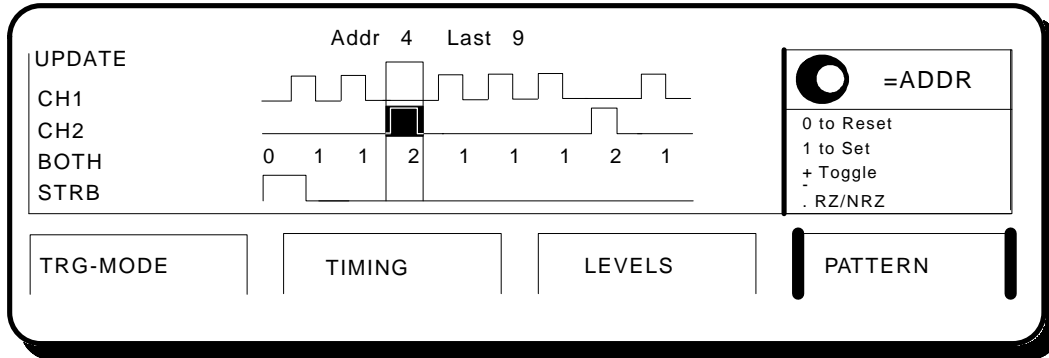
1	OFF	Per	33.3ns	2	<input checked="" type="radio"/> MODIFY 20.0 ns
Delay	10.0ns	Delay	0.00ns	Width	
Width	10.0ns	Width	20.0ns	LeadEdg	2.00ns
LeadEdg	2.00ns	LeadEdg	2.00ns	TrailEd	2.00ns
TrailEd	2.00ns	TrailEd	2.00ns		
TRG-MODE	TIMING	LEVELS	PATTERN		

UPDATE	Addr	4	Last	9	<input checked="" type="radio"/> =ADDR 0 to Reset 1 to Set + Toggle . RZ/NRZ				
CH1	0	1	1	0		1	1	1	0
CH2	0	0	0	1	0	0	0	1	0
BOTH	0	1	1	2	1	1	1	2	1
STRB	1	0	0	0	0	0	0	0	0
TRG-MODE	TIMING	LEVELS	PATTERN						

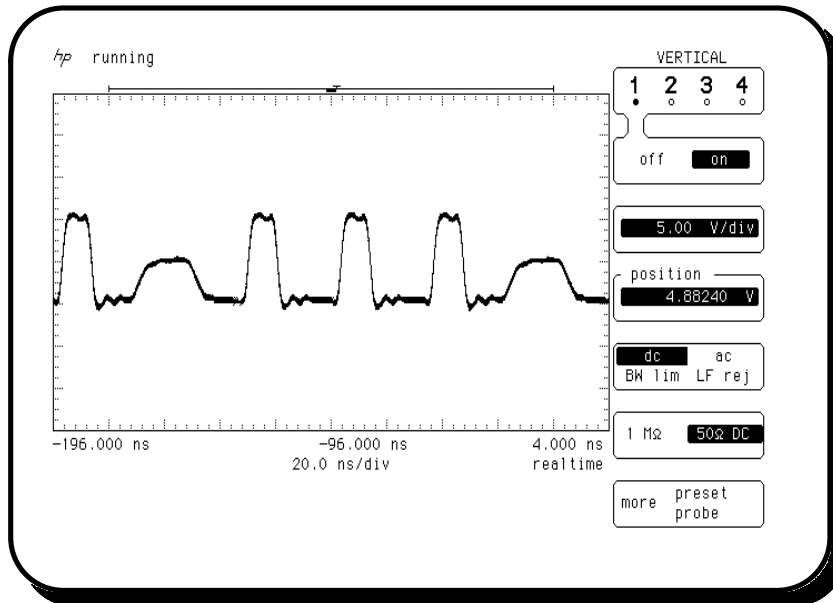
4. Set up the following bit pattern in the **PATTERN** menu.

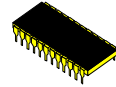


5. Press the PATTERN key again to view the pulses.



6. Here is the HP 54542A Scope display of the Write and Erase pulses generated by adding the HP 8110A channels together at output 1.





## Simulating Noise Signals for Tolerance Testing

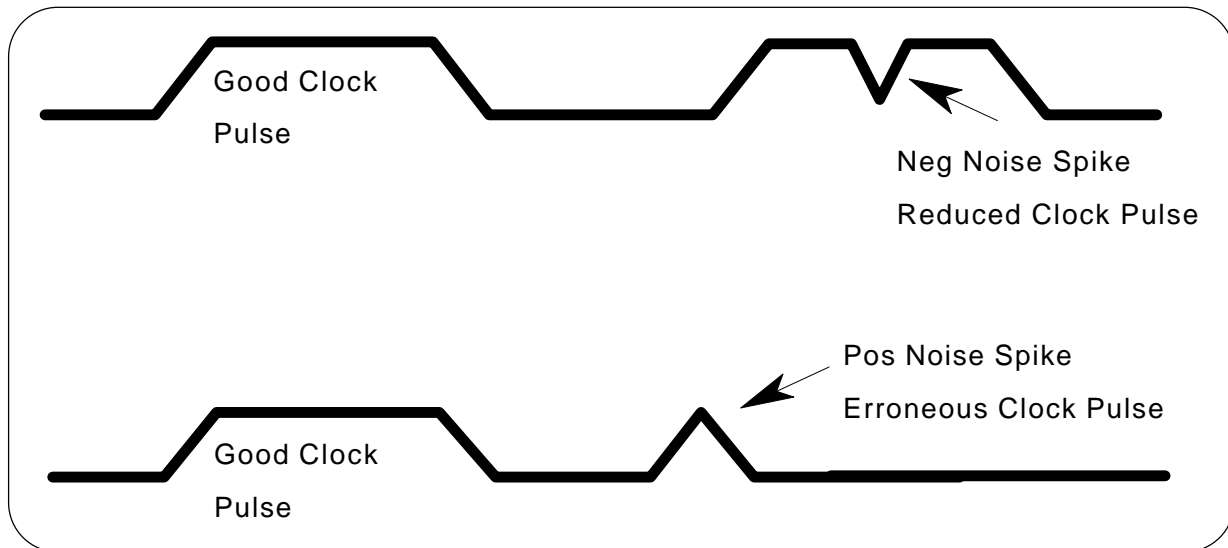
**Industry/Application Area:**  
Computer/R&D

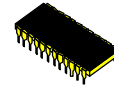
### Overview:

Computer memory elements, such as flip-flops and memory cells, require a clock pulse (or a write strobe) to change the device state once the new data has been presented. Noise in the clock signal may be seen as a valid clock by the device or degrade a good clock pulse so the device never sees it.

To insure accuracy and reliability in a design, the designer must minimize noise sources that can cause system failures. However, it is not always cost effective to eliminate all sources of noise, so the designer needs a way to judge the effects of noise on particular circuits. In the past, it has been difficult to simulate noise in a way that is stable and repeatable (so that the noise effects could be judged objectively).

### Simulated Noise Spikes:





### Setting up the HP8110A for a negative noise spike:

1. Using the MODIFY knob select PATTERN mode in the TRG-MODE menu.

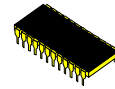
CONTINUOUS <b>PATTERN of</b>		<input checked="" type="radio"/> MODIFY PulseStrm Burst *Pattern	
NRZ-Pulses at Out1 NRZ-Pulses at Out2			
Pulse-Period: internal Osc			
TRG-MODE	TIMING	LEVELS	PATTERN

2. Then select RZ-PULSES AT OUT 1 & 2.

CONTINUOUS PATTERN of		<input checked="" type="radio"/> MODIFY * RZ NRZ	
<b>RZ-Pulses at Out1</b> RZ-Pulses at Out2			
Pulse-Period: internal Osc			
TRG-MODE	TIMING	LEVELS	PATTERN

3. Now go to the LEVELS Menu, COMPLEMENT Channel 2 and add the channels together.

Normal		Complmnt		<input checked="" type="radio"/> MODIFY Seperate *Added
1 OFF	<b>Added at Output 1</b>		2	
High +2.50V Low +0.0mV 48 Ω into 50.0 Ω	High +0.0mV Low -800mV			
TRG-MODE	TIMING	LEVELS	PATTERN	



4. Set all of the parameters as shown below in the TIMING menu.

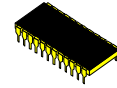
1	OFF	Per	33.3ns	2	<input type="radio"/> MODIFY
Delay	0.00ns	Delay	0.00ns	5.00 ns	
Width	20.0ns	Width	5.00ns		
LeadEdg	5.00ns	LeadEdg	2.00ns		
TrailEd	5.00ns	TrailEd	2.00ns		
TRG-MODE		TIMING		LEVELS	
				PATTERN	

5. Set up the following pattern in the PATTERN menu.

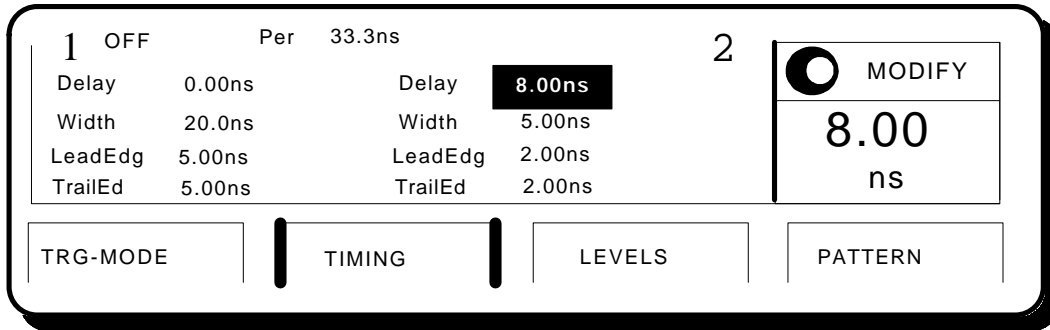
UPDATE	Addr	5	Last	10	<input type="radio"/> = ADDR				
CH1	1	0	1	0	1	0	1	0	
CH2	1	0	0	0	0	0	0	0	0
BOTH	3	0	1	0	1	0	1	0	1
STRB	1	0	0	0	0	0	0	0	0
TRG-MODE		TIMING		LEVELS		PATTERN			

6. Press the PATTERN Menu key again to view the waveforms.

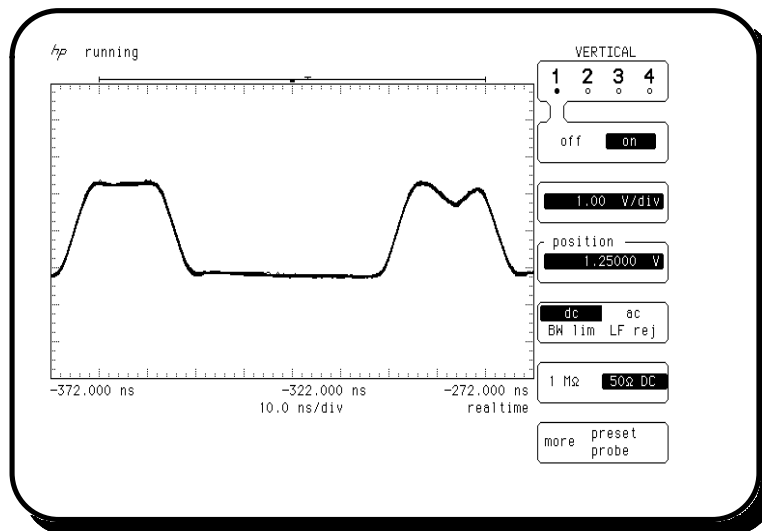
UPDATE	Addr	5	Last	10	<input type="radio"/> = ADDR				
CH1									
CH2									
BOTH	3	0	1	0	1	0	1	0	1
STRB									
TRG-MODE		TIMING		LEVELS		PATTERN			

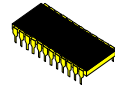


7. Go to the TIMING menu and adjust channel 2 delay to position the negative noise spike.



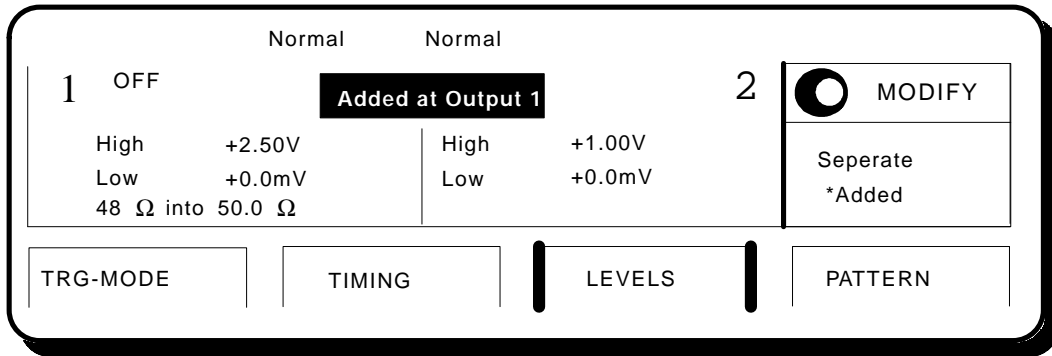
8. Here is the HP 54542A Scope display of the negative noise spike on channel 2 added to the positive pulses on channel 1 from the HP 8110A.



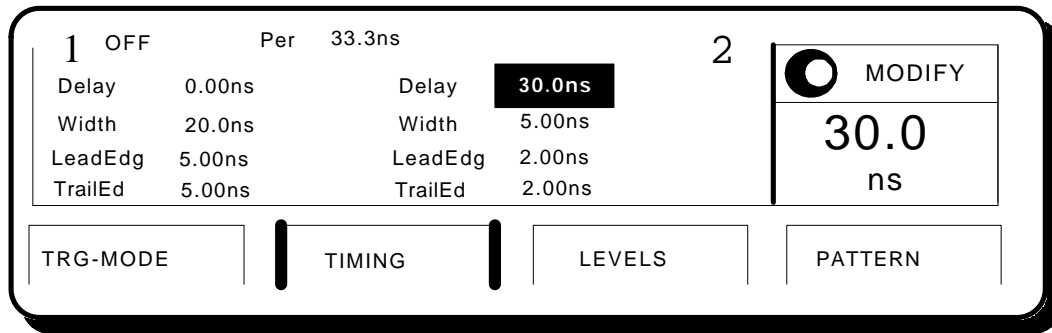


Setting up the HP 8110A for a positive noise spike:

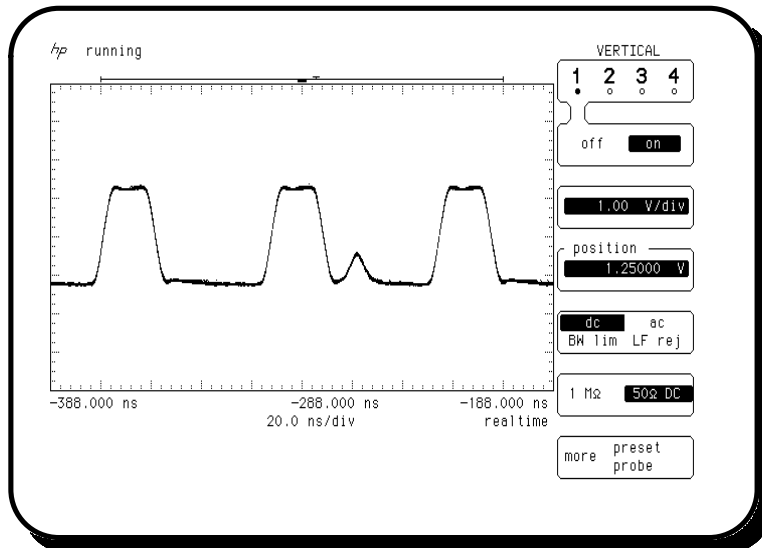
- 1. Change the levels as shown below and make sure they are still added together in the LEVELS menu.



- 2. Go to the TIMING menu and set channel 2 delay to 30.0 ns.



- 3. Here is the HP 54542A Scope display of the positive noise spike generated from the HP 8110A.







## Simulation of Distorted Video Signals



### Industry/Application Area:

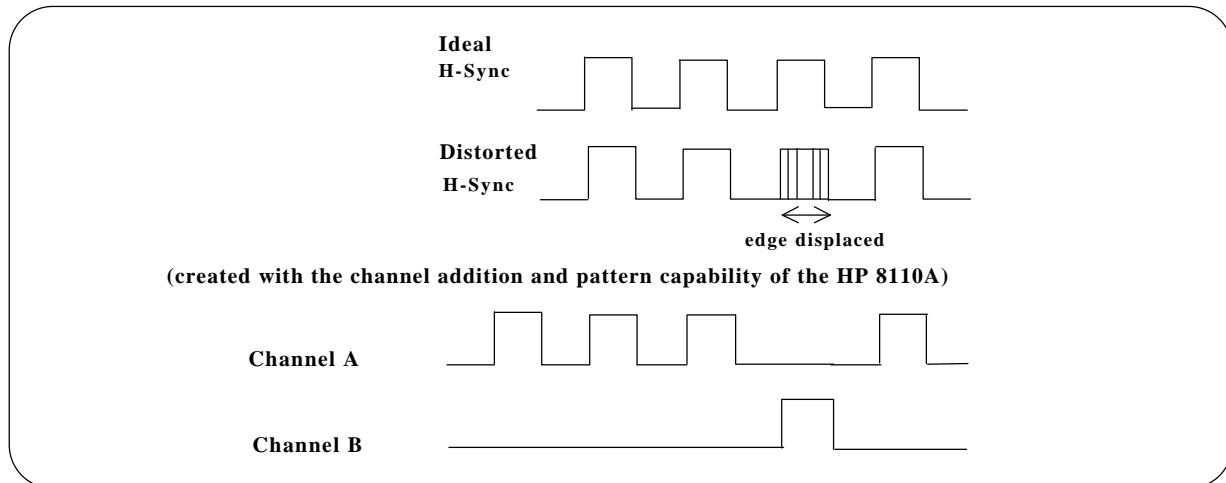
Communications/R&D of Video Interfaces for Projection Units

### Overview:

Several data communication companies develop interfaces between LCOs (Local Clock Oscillators) and Video/TV/Computers for overhead projection units. It is very important for them to stay up-to-date with the rapidly changing video interfaces in computers, and to have test equipment that can simulate these different interfaces, (such as 1024X768 pixels and HDTV interfaces). These interfaces vary from 33 MHz to 80 MHz.

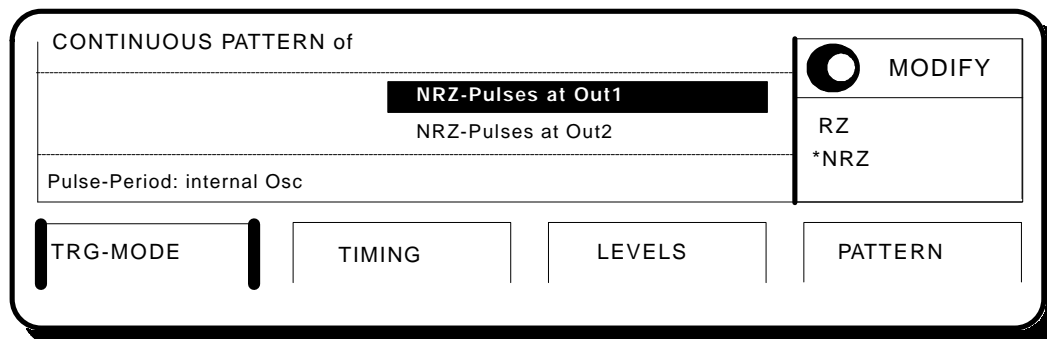
A critical indicator of the quality of their design is it's sensitivity to distorted video signals, (both in amplitude and frequency jitter).

### Timing Diagram of Horizontal Sync Jitter:



### Setting up the HP 8110A :

1. Select NRZ Pulses in the TRG-MODE menu using the MODIFY knob.





2. Set up the bit pattern as shown below in the PATTERN menu.

UPDATE	Addr 5	Last 8
CH1	1 0 1 0	0 0 1 0
CH2	0 0 0 0	1 0 0 0
BOTH	1 0 1 0	2 0 1 0
STRB	1 0 0 0	0 0 0 0

= ADDR  
 0 to Reset  
 1 to Set  
 + Toggle  
 - RZ/NRZ

TRG-MODE

TIMING

LEVELS

PATTERN

3. Press the PATTERN key again to view the waveforms.

UPDATE	Addr 4	Last 8
CH1		
CH2		
BOTH	1 0 1 0	2 0 1 0
STRB		

= ADDR  
 0 to Reset  
 1 to Set  
 + Toggle  
 - RZ/NRZ

TRG-MODE

TIMING

LEVELS

PATTERN

4. Go to the LEVELS Menu to add the channels together.

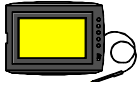
1	OFF	Normal	Normal	OFF	2
		Added at Output 1			<input type="radio"/> MODIFY
	High	+1.00V	High	+1.00V	Seperate
	Low	+0.0mV	Low	+0.0mV	*Added
	48 Ω into	50.0 Ω			

TRG-MODE

TIMING

LEVELS

PATTERN

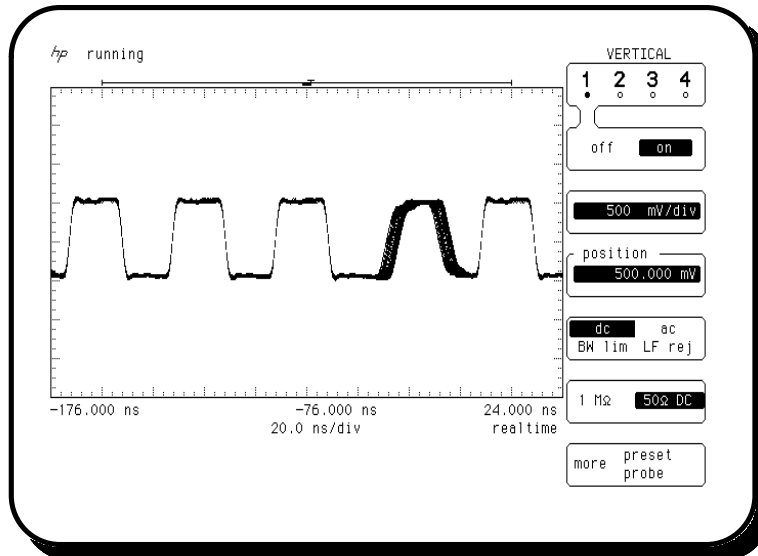


5. Vary channel 2 DELAY to jitter the pulse.

1	OFF	Per	20.0ns	2	<input checked="" type="radio"/> MODIFY
Delay	0.00ns	Delay	<b>5.00ns</b>		<b>5.00</b>
Width	-----	Width	-----		ns
LeadEdg	2.00ns	LeadEdg	2.00ns		
TrailEd	2.00ns	TrailEd	2.00ns		

TRG-MODE
TIMING
LEVELS
PATTERN

6. Here is the HP 54542A Scope display of the "jittering" pulse generated by the HP 8110A.





## Radar Distance Test to Airborne Planes

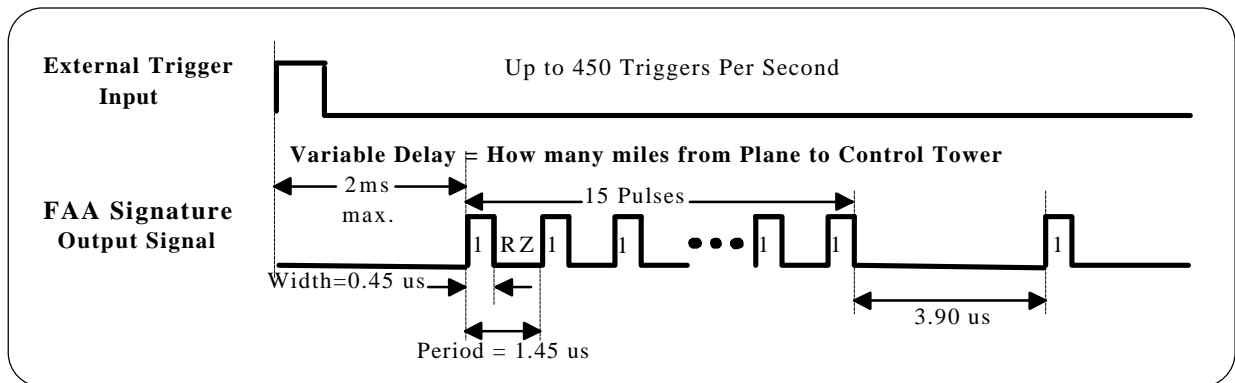
### Industry/Application Area:

Aerospace/Radar Communications

### Overview:

A trigger pulse train of double pulses is sent from the control tower's radar system to an airborne plane. The plane responds with a standard signature signal which is sent back to the control tower. This occurs up to 450 times per second. The control tower receives the signal, recognizes its signature, and then analyzes the delay to determine the distance of the airborne plane from the control tower. The FAA (USA's Federal Aviation Administration) requires the radar system to be tested on a regular basis. An HP 8110A can be used to simulate the signature signal by using it in pattern mode and can also simulate varying distances from the control tower by varying the delay from the external trigger signal to the start of the output signal. Due to the legal safety requirements, it is critical to have very accurate edge placement of the pulses in the signature signal. The edge placement accuracy is improved 50 times by adding the HP 81106A module.

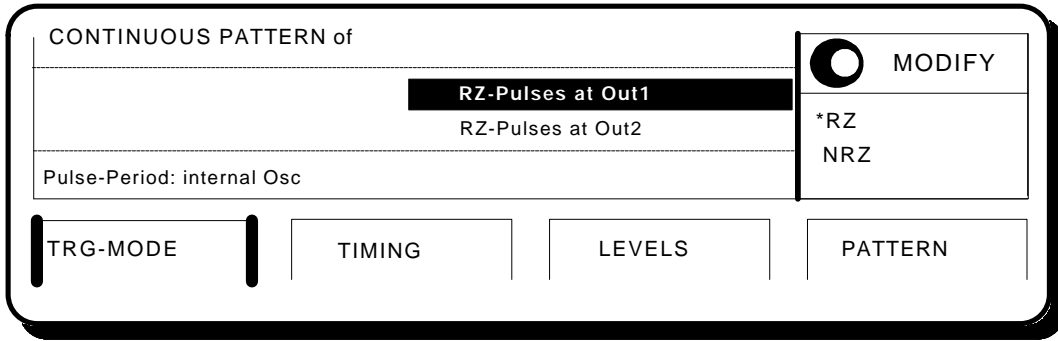
### Timing Diagram of Standard FAA Output Signal:



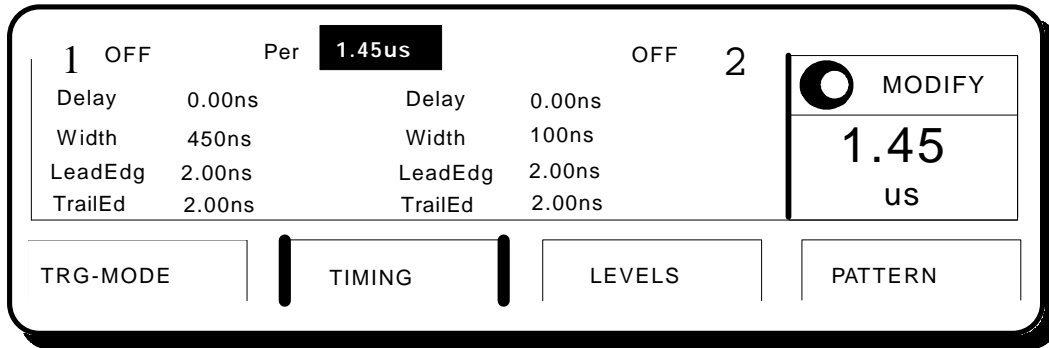


**Setting up the HP 8110A:**

1. Select **RZ-PULSES AT OUT 1** in the **TRG-MODE** menu.



2. Then go to the **TIMING** menu and set the **PERIOD** and pulse **WIDTH** specified in the timing diagram





3. In order to get the 2.0 ms delay we need to add leading zeros to the 18 bit pattern (the HP 8110A will not allow us to ask for more than 1.37 us delay). With the RZ pulses set at 1.45 us period we need 1,379 leading zeros. That will give us 1,999.55us of delay. To get these leading zeros go to the PATTERN menu. Set the last address to be 1397 (1,379 + 18 bit pattern) then select FILL 0, ENTER.

UPDATE	Addr	1	Last	1397
CH1	0	0	0	0
CH2	0	0	0	0
BOTH	0	0	0	0
STRB	1	0	0	0

+ENTER

\* Fill 0

Fill 1

Invert

First Bit

TRG-MODE
TIMING
LEVELS
PATTERN

4. Now starting at address 1379 set the 18 bit pattern of the radar signal.  
 Note: The pattern is consecutive "1"s from address 1379 to 1394.

UPDATE	Addr	1391	Last	1397
CH1	1	1	1	1
CH2	0	0	0	0
BOTH	1	1	1	1
STRB	1	0	0	0

= ADDR

0 to Reset

1 to Set

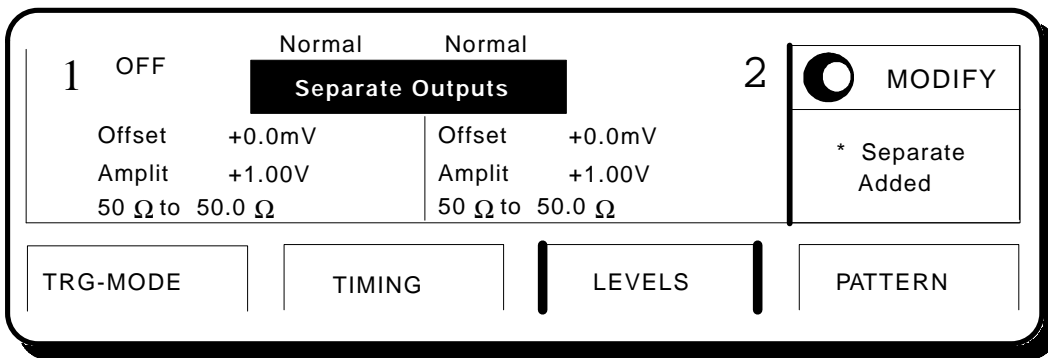
+ Toggle

. RZ/NRZ

TRG-MODE
TIMING
LEVELS
PATTERN



5. Finally, go to the LEVELS Menu to set up the voltages and select SEPARATE OUTPUTS.



6. Here is the HP 54542A Scope display of the last 14 pulses of the FAA Signature Output Signal generated by the HP 8110A.

